12-17-99

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

A

In re Application of : Sheldon Aronowitz et. al.

For : Process for Etching a Controllable Thickness of Oxide On An Integrated Circuit Structure On A Semiconductor Substrate Using Nitrogen Plasma and an RF Bias Applied to the Substrate

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Maria Kovacs

DEC. 15, 1999 Date

Maria Kovacs Signature

Atty Docket : 99-039

jc715 U.S. PTO 12/15/99

jc675 U.S. PTO 09/464297 12/15/99

TRANSMITTAL LETTER FOR PATENT APPLICATION

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir,

The following paper(s) and/or fee(s) are being deposited with the United States Postal Service "Express Mail Post Office to Addressee", addressed to :

Box Patent Application
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1. Fee Transmittal Form (in duplicate).
2. Patent Application comprising the following :

   a. Specification, pages = 11

   b. Drawing, sheets = 1

   c. Assignment and declaration with power of attorney.

It is respectfully requested that the Commissioner accord the enclosed patent application a filing date and a serial number.

If it is determined that any additional fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 12-2252.

LSI Logic Corporation
1551 McCarthy Blvd., MS D-106
Milpitas, CA 95035
408/433-8708

Date: 12/15/99

Respectfully submitted,

Ralph R. Veseli

Ralph Veseli

Reg. No. 33,807

PROCESS FOR ETCHING A CONTROLLABLE THICKNESS OF OXIDE ON AN INTEGRATED CIRCUIT STRUCTURE ON A SEMICONDUCTOR SUBSTRATE USING NITROGEN PLASMA AND AN RF BIAS APPLIED TO THE SUBSTRATE

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to a process for use in the construction of integrated circuit structures. More particularly, this invention relates to a process for etching an accurate thickness of oxide from an oxide surface of an integrated circuit structure on a semiconductor substrate using a nitrogen plasma and a rf bias applied to the substrate.

2. Description of the Related Art

In the construction of an integrated circuit structure on a semiconductor substrate, an oxide material, such as silicon oxide, is the material of choice for providing insulation or dielectric material between electrically conductive portions of the integrated circuit structure. The silicon oxide insulation material is normally formed as an oxide layer over other portions of the integrated circuit structure, and the oxide layer may then be subsequently patterned to form the desired shape. Alternatively, portions of oxide may be individually formed over segments of the underlying integrated circuit structure using masks to isolate such portions of oxide from the remainder of the integrated circuit structure, e.g., the formation of field oxide between transistor areas. In either case, the formation of the oxide on the integrated circuit structure is usually carried out either by deposition of silicon oxide on the integrated circuit structure, e.g., by chemical vapor deposition (CVD); or by growth of the silicon oxide, e.g., growth of silicon oxide on an exposed silicon surface, e.g., by oxidation of the silicon using water vapor.

As integrated circuit structures have continued to shrink, both in size of individual components as well as in spacing between such components, it has become necessary to accurately control the thickness of such silicon oxide portions formed on the integrated circuit structures. For example, formation of an MOS transistor may require the formation of a high quality gate oxide of less than 2.5 nanometers (nm) in thickness. This formation of very thin oxide layers

has become increasingly difficult to accomplish using conventional deposition or growth processes when thin oxide layers of accurate and uniform thickness are required.

It would, therefore, be useful to provide a process for the accurate and reproducible removal of controlled thicknesses of silicon oxide from a previously formed silicon oxide portion or layer of an integrated circuit structure on a semiconductor substrate.

SUMMARY OF THE INVENTION

In accordance with the invention, a reproducibly accurate and uniform amount of silicon oxide can be removed from the surface of an oxide previously formed over a semiconductor substrate by exposing the oxide to a nitrogen plasma in an etch chamber while applying an rf bias to a substrate support on which the substrate is supported in an etch chamber. The thickness of the silicon oxide removed in a given period of time may be changed by changing the amount of rf bias applied to the substrate through the substrate support.

BRIEF DESCRIPTION OF THE DRAWINGS

The sole figure is a flow sheet illustrating the process of the invention.

DETAILED DESCRIPTION OF THE INVENTION

The invention comprises a process for removing a reproducibly accurate and uniform amount of oxide from an oxide surface of an oxide portion or layer previously formed on an integrated circuit structure over a semiconductor substrate. The process comprises exposing the oxide to a nitrogen plasma in an etch chamber while applying an rf bias to a substrate support on which the substrate is supported in the etch chamber. The thickness of the oxide removed in a given period of time may be changed by changing the power level of the rf bias applied to the substrate through the substrate support. In one embodiment, the nitrogen plasma used to remove the oxide may comprise a remote plasma.

In accordance with the invention, the rf bias applied to the substrate through the substrate support during the oxide etch may comprise an rf bias from an rf power source such as, for example, a 13.56 MHz rf power source. The power level, which in the process of the invention is used to control the thickness of silicon oxide removed during any given etch time period, may range from as small as slightly above zero to a maximum rf bias power level below a power level at which implanting of the substrate would occur. Typically the rf bias power applied to the substrate support will range from just above zero to a maximum of about 100 watts, with rf bias power levels ranging from about 10 watts to about 50 watts being most frequently used.

With respect to the minimum rf bias power level of just slightly above zero, it should be noted that at zero bias power level, the nitrogen plasma can be used for nitridation of the substrate, rather than for etching purposes, and such nitridation can be carried out at zero bias level without sputtering. This capability of nitridation of the oxide on the substrate at zero bias is an advantage because the control of the minimum etch rate (by control of the rf bias power on the substrate) can be maintained to a degree impossible with any wet etch source, since the incorporation of nitrogen into the oxide due to nitridation at zero bias level would be beneficial to some degree, rather than detrimental, e.g., for reducing boron penetration into gate oxide from a polysilicon gate. When it is desired to conduct a deliberate nitridation of the remaining oxide after the oxide etch of the invention, the rf bias on the substrate support may be simply turned off without, however, extinguishing the plasma and then maintaining the plasma in the etch chamber for the desired period of time to carry out the nitridation.

The etch is carried out while maintaining a pressure within the etch chamber sufficient to permit maintenance of a plasma in the etch chamber, yet low enough to avoid damage to the system and to maintain the pressure within the capabilities of the system. Preferably, the pressure will be maintained within a range of from about 1 millitorr to about 1000 millitorr, and most preferably from about 1 millitorr to about 500 millitorr, with pressures ranging from about 1 millitorr to about 100 millitorr being typical. Maintaining the pressure in the etch chamber within these ranges will usually satisfy the above criteria. It should be noted that the higher the pressure, the longer the etch time will be extended for removal of a given thickness of oxide because of the increase in recombination of ions with increased pressure. The flow

of the gaseous source of nitrogen into the chamber will be related to the desired pressure maintained within the chamber and the pumping speed of the apparatus.

The nitrogen plasma in the etch chamber is established by flowing a gaseous source of nitrogen, such as N_2 or another nitrogen-containing gas such as N_2O or NO, into the etch apparatus and igniting the plasma, using an rf plasma power source maintained within a power range of from a minimum power capable of maintaining the plasma in the etch chamber up to a maximum power level which will not damage either the equipment or the substrate. Maintaining the plasma power source within a power range of from about 250 watts to about 1000 watts will satisfy these criteria. Preferably, the power level will be maintained within a range of from about 250 watts to about 500 watts. Within such a plasma power range, it has been found that the oxide removal rate is independent of the plasma power level.

The temperature at which the etch is carried out is not considered to be crucial, except that maximum temperatures should be below temperatures which might damage the etching apparatus or other portions of the integrated circuit structure on the semiconductor substrate. Temperatures below about 250°C should be sufficient from a standpoint of equipment damage. However, lower maximum temperatures, such as 60°C or less, may be preferable from a standpoint of damage to the integrated circuit structure, such as resist masks present on the structure during the etching. Thermal budget requirements may also favor the use of lower maximum temperatures during the etch. In any event, for preserving the reproducible characteristics of the etch, it is preferable that a single operating temperature within the above considerations be selected for conduct of the oxide etch process.

By use of the term "remote plasma" is meant a plasma which is generated at a distance from the substrate target sufficiently far enough from the plasma origin that recombination of at least some of the electrons with the ionic nitrogen species occurs so that the flux of ionic species will be reduced from the initial flux created at the plasma's origin. Etching apparatus having such remote plasma generation capabilities are commercially available, such as, for example, a LAM 9400SE Transformer Coupled Plasma (TCP) reactor or an Applied Materials DPS reactor.

It should be noted that the purpose of the rf bias on the substrate support is to provide a charged electrode which will accelerate and control the flow of the components of the nitrogen plasma toward the substrate to obtain the desired etching of an accurate and reproducible amount of oxide from the substrate. With this in mind, in another embodiment of the invention, a triode reactor apparatus could also be used wherein a charged grid in the apparatus would serve as the charged electrode, instead of (or supplementary to) the biased substrate support, to accelerate and control the flow of the components of the nitrogen plasma toward the surface of the substrate. Such triode reactor apparatus are commercially available, for example, from the LAM company as Model No. 9500.

The oxide etch may be carried out selectively on particular unmasked oxide regions while other masked oxide regions are not etched, e.g., to form very thin gate oxide portions. Alternatively, the oxide etching process of the invention may be used for uniform thinning of a blanket deposited layer of oxide where deposition controls alone are inadequate to accurately and reproducibly form a thin oxide layer of uniform thickness.

To further illustrate the practice of the process of the invention, 4.5 nanometers (nm) of silicon oxide was grown on an eight inch diameter silicon substrate. The substrate was then masked and each of three quadrants of the substrate were sequentially exposed to a nitrogen plasma while an rf bias was applied to the substrate support at respective rf bias power levels of 15 watts during etching of the first quadrant, 25 watts during etching of the second quadrant, and 40 watts during etching of the third quadrant, with the fourth quadrant remaining masked as a control. The substrate-biased nitrogen plasma etch of the invention was carried out in a LAM 9400SE TCP remote plasma reactor in which the etch chamber was maintained at a pressure of 40 millitorr and a temperature of about 60°C, with the plasma generator power level maintained at about 500 watts. For each quadrant on the substrate, the oxide etch was carried out for 18 seconds. The respective thicknesses of the control and the oxide layers in each quadrant of the substrate after the respective etches were measured by ellipsometry at 9 points using a Rudolph FEIII Ellipsometer. The minimum, maximum, and average thicknesses of the oxide for the control quadrant and the quadrant subject to the 40 watt bias were determined and are tabulated below.

TABLE

Bias Power	Average Thickness (nm)	Minimum Measured Thickness (nm)	Minimum Measured Thickness (nm)
Control	4.617	4.603	4.627
40 Watts	1.689	1.674	1.696

Similar consistency in uniform thickness removal were noted for the quadrants subject respectively to etching with the 15 watt and 25 watt bias on the substrate support.

The same experiment was carried out with the plasma power level reduced to 250 watts, with all other parameters remaining constant. The results indicated that reduction of the plasma power level to 250 watts did not materially change the etch behavior, indicating that for a given etch time period, it is the bias power which determines the oxide etch rate for any given time period.

Thus, it can be seen that the oxide etch process of the invention is capable of removing a uniform thickness of oxide from an oxide layer or portion in a nitrogen plasma etch process by maintaining a particular power level of rf bias on the substrate during the etch, with the thickness of the removed silicon oxide during any given time period varying with the power level of the rf bias maintained on the substrate during the nitrogen plasma etch.

Having thus described the invention what is claimed is:

1. A process for etching away a fixed thickness of silicon oxide in an integrated circuit structure on a semiconductor substrate in an etching chamber which comprises:

a) exposing an oxide surface of said integrated circuit structure on said semiconductor substrate in said etching chamber to a nitrogen plasma; and

b) maintaining, on an electrode in said etching chamber, a bias at a predetermined power level during said exposure of said oxide surface to said nitrogen plasma to control the flow of components of said nitrogen plasma toward said substrate;

whereby a fixed thickness of silicon oxide will be removed from said oxide surface, with the oxide thickness removed dependent upon said power level of said bias on said electrode in said etching chamber.

2. The process for etching away a fixed thickness of silicon oxide of claim 1 wherein said electrode comprises a substrate support in said etching chamber.

3. The process for etching away a fixed thickness of silicon oxide of claim 1 wherein said electrode comprises an electrically conductive grid in said etching chamber.

4. A process for etching away a fixed thickness of silicon oxide in an integrated circuit structure on a semiconductor substrate in an etching apparatus which comprises:

a) exposing an oxide surface of an integrated circuit structure on a semiconductor substrate to a nitrogen plasma; and

b) maintaining an rf bias at a predetermined power level on said semiconductor substrate during said exposure of said oxide surface to said nitrogen plasma;

whereby a fixed thickness of silicon oxide will be removed from said oxide surface, with the oxide thickness removed dependent upon said power level of said rf bias on said semiconductor substrate.

5. The process for etching away a fixed thickness of silicon oxide of claim 4 wherein said nitrogen plasma is formed by flowing a gas containing nitrogen into said etching apparatus, and then igniting said nitrogen plasma in said etching apparatus.

6. The process for etching away a fixed thickness of silicon oxide of claim 4 wherein said nitrogen plasma is maintained at a power level of from about 250 watts to about 1000 watts.

7. The process for etching away a fixed thickness of silicon oxide of claim 4 wherein said nitrogen plasma comprises a remote plasma.

8. The process for etching away a fixed thickness of silicon oxide of claim 4 wherein said power level of said rf bias on said substrate ranges from above zero up to a power level just below a level at which sputtering of said substrate materials would commence.

9. The process for etching away a fixed thickness of silicon oxide of claim 4 wherein said etching process is carried out in an etching chamber in said etching apparatus maintained at a pressure of from about 1 millitorr to about 1000 millitorr.

10. The process for etching away a fixed thickness of silicon oxide of claim 4 wherein said oxide surface exposed to said nitrogen plasma comprises an oxide layer previously formed on said integrated circuit structure.

11. A process for etching away a fixed thickness of silicon oxide in an integrated circuit structure on a semiconductor substrate mounted on a substrate support in an etching chamber of an etching apparatus which comprises:

a) exposing an oxide surface of an integrated circuit structure on a semiconductor substrate to a nitrogen plasma formed by flowing a gas containing nitrogen into said etching apparatus, and then igniting a plasma in said etching apparatus; and

b) maintaining, on said substrate support, during said exposure of said oxide surface to said nitrogen plasma, an rf bias at a power level ranging from above zero up to a power level just below a level at which sputtering of said substrate materials would commence;

whereby a fixed thickness of silicon oxide will be removed from said oxide surface, with the oxide thickness removed dependent upon said power level of said rf bias on said substrate support.

12. The process for etching away a fixed thickness of silicon oxide of claim 11 wherein said power level of said rf bias on said substrate support ranges from above zero up to about 100 watts.

13. The process for etching away a fixed thickness of silicon oxide of claim 11 wherein said nitrogen plasma is maintained at a power level of from about 250 watts to about 500 watts.

14. The process for etching away a fixed thickness of silicon oxide of claim 11 wherein said nitrogen plasma comprises a remote plasma.

15. The process for etching away a fixed thickness of silicon oxide of claim 11 wherein said etching chamber is maintained at a pressure of from about 1 millitorr to about 500 millitorr.

16. The process for etching away a fixed thickness of silicon oxide of claim 11 wherein said oxide surface exposed to said nitrogen plasma comprises an oxide layer previously formed on said integrated circuit structure.

17. The process for etching away a fixed thickness of silicon oxide of claim 11 wherein said oxide surface exposed to said nitrogen plasma comprises unmasked portions of an oxide layer previously formed on said integrated circuit structure.

18. The process for etching away a fixed thickness of silicon oxide of claim 11 wherein said oxide surface exposed to said nitrogen plasma comprises a surface of one or more oxide portions previously formed on said integrated circuit structure.

19. A process for etching away a fixed thickness of silicon oxide in an integrated circuit structure on a semiconductor substrate which comprises:

a) placing said semiconductor substrate on a substrate support in an etching chamber of an etching apparatus, said chamber maintained at a pressure of from about 1 millitorr to about 500 millitorr;

b) exposing an oxide surface of an integrated circuit structure on a semiconductor substrate to a nitrogen plasma maintained at a power level of from about 250 watts to about 500 watts and formed by flowing a gas containing nitrogen into said etching apparatus, and then igniting a plasma in said etching apparatus; and

c) maintaining, on said substrate support, during said exposure of said oxide surface to said nitrogen plasma, an rf bias at a power level ranging from above zero up to about 100 watts;

whereby a fixed thickness of silicon oxide will be removed from said oxide surface, with the oxide thickness removed dependent upon said power level of said rf bias on said semiconductor substrate.

20. The process for etching away a fixed thickness of silicon oxide of claim 19 wherein said power level of said rf bias on said substrate ranges from above zero up to about 50 watts.

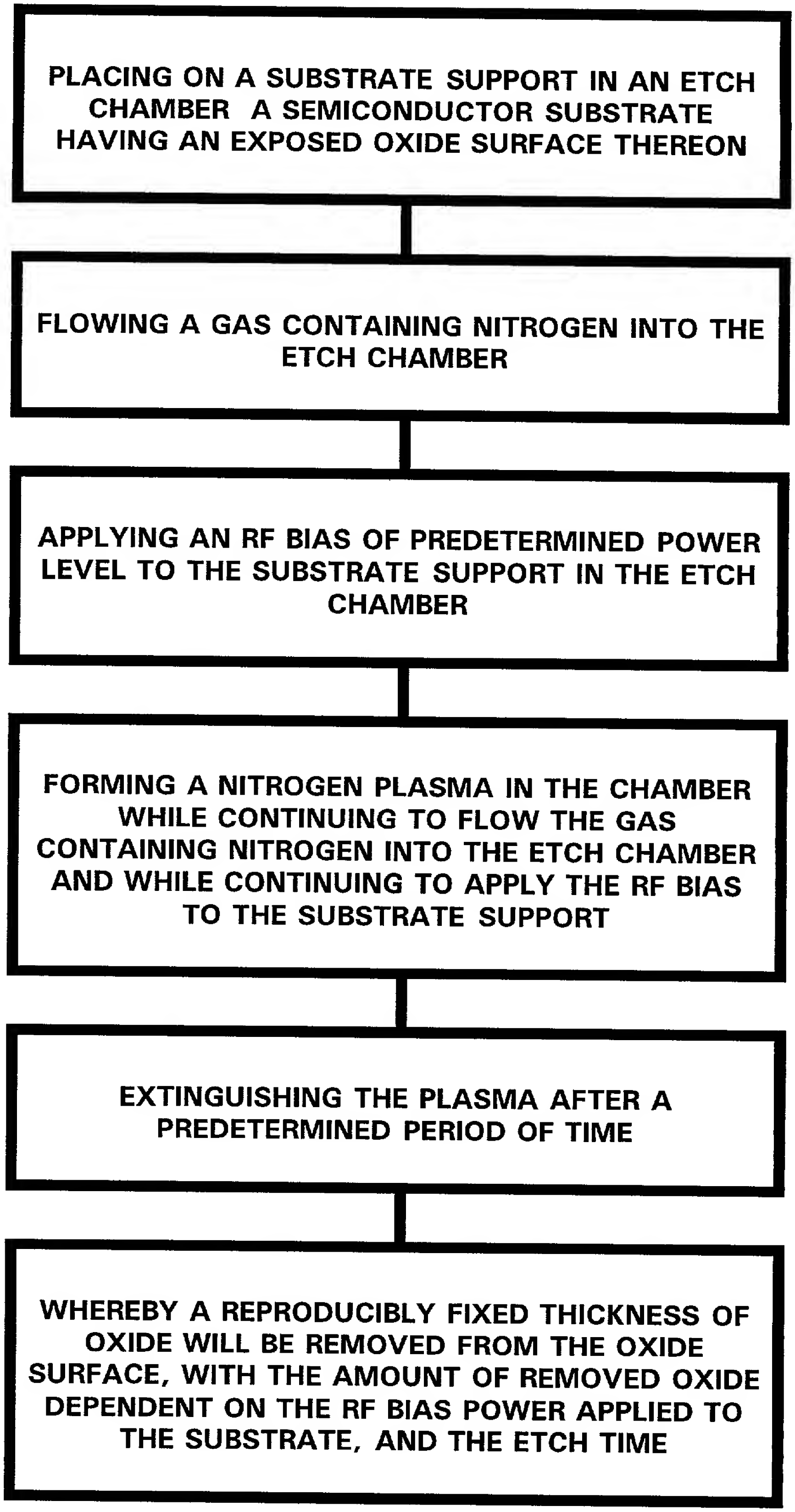
21. The process for etching away a fixed thickness of silicon oxide of claim 19 wherein said oxide surface exposed to said nitrogen plasma comprises an oxide layer previously formed on said integrated circuit structure.

22. The process for etching away a fixed thickness of silicon oxide of claim 19 wherein said etching chamber is maintained at a pressure of from about 1 millitorr to about 200 millitorr.

23. The process for etching away a fixed thickness of silicon oxide of claim 19 wherein said nitrogen plasma comprises a remote plasma.

ABSTRACT OF THE INVENTION

A process for etching oxide is disclosed wherein a reproducibly accurate and uniform amount of silicon oxide can be removed from a surface of an oxide previously formed over a semiconductor substrate by exposing the oxide to a nitrogen plasma in an etch chamber while applying an rf bias to a substrate support on which the substrate is supported in the etch chamber. The thickness of the oxide removed in a given period of time may be changed by changing the amount of rf bias applied to the substrate through the substrate support.


PLACING ON A SUBSTRATE SUPPORT IN AN ETCH CHAMBER A SEMICONDUCTOR SUBSTRATE HAVING AN EXPOSED OXIDE SURFACE THEREON
FLOWING A GAS CONTAINING NITROGEN INTO THE ETCH CHAMBER
APPLYING AN RF BIAS OF PREDETERMINED POWER LEVEL TO THE SUBSTRATE SUPPORT IN THE ETCH CHAMBER
FORMING A NITROGEN PLASMA IN THE CHAMBER WHILE CONTINUING TO FLOW THE GAS CONTAINING NITROGEN INTO THE ETCH CHAMBER AND WHILE CONTINUING TO APPLY THE RF BIAS TO THE SUBSTRATE SUPPORT
EXTINGUISHING THE PLASMA AFTER A PREDETERMINED PERIOD OF TIME
WHEREBY A REPRODUCIBLY FIXED THICKNESS OF OXIDE WILL BE REMOVED FROM THE OXIDE SURFACE, WITH THE AMOUNT OF REMOVED OXIDE DEPENDENT ON THE RF BIAS POWER APPLIED TO THE SUBSTRATE, AND THE ETCH TIME

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Attorney Docket No.: **99-039**

PATENT

DECLARATION, POWER OF ATTORNEY, AND PETITION

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled "PROCESS FOR ETCHING A CONTROLLABLE THICKNESS OF OXIDE ON AN INTEGRATED CIRCUIT STRUCTURE ON A SEMICONDUCTOR SUBSTRATE USING NITROGEN PLASMA AND AN RF BIAS APPLIED TO THE SUBSTRATE", the specification of which:

_X_ is attached hereto.
_____ was filed on _____ as Application Serial No. _____, and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, § 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

PRIOR FOREIGN APPLICATION(S)			Priority Claimed
_____			Yes ___ No ___
(Number)	(Country)	(Date Filed)	
_____			Yes ___ No ___
(Number)	(Country)	(Date Filed)	

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a), regarding events which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status)
(Application Serial No.)	(Filing Date)	(Status)

I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

I hereby appoint John P. Taylor, Reg. 22,369; David G. Pursel, Reg. 28,659; Ralph R. Veseli, Reg. 33,807; Bruce R. Hopenfeld, Reg. 39,714; Sandeep Jaggi, Reg. 43,331; and Gary Edward Ross, Reg. 29,431; as my attorneys with full power of substitution and revocation, to prosecute this application and to transact all business in the U.S. Patent and Trademark Office connected therewith and before competent international authorities.

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Please send all correspondence to:

Ralph R. Veseli, Patent Attorney
Intellectual Property Law Department
LSI Logic Corporation
M/S D-106
1551 McCarthy Boulevard
Milpitas, CA 95035
(408) 433-6404

Wherefore I pray that Letters Patent be granted to me for the invention or discovery described and claimed in the foregoing specification and claims, and I hereby subscribe my name to the foregoing specification and claims, declaration, power of attorney, and this petition.

First Inventor's Full Name: Sheldon (First) (Initial) Aronowitz (Last)

Inventor's Signature: _____

Date: DECEMBER 7, 1999 Country of Citizenship: USA

Residence Address: San Jose, California

Post Office Address: 3577 Barley Court, San Jose, CA 95127-4401 USA

Second Inventor's Full Name: Valeriy (First) (Initial) Sukharev (Last)

Inventor's Signature: Valeriy Sukharev

Date: December 7, 1999 Country of Citizenship: USA

Residence Address: Cupertino, California

Post Office Address: 11476 Garden Terrace Drive, Cupertino, CA 95014 USA

Third Inventor's Full Name: John (First) (Initial) Haywood (Last)

Inventor's Signature: JHaywood

Date: December 8th 1999. Country of Citizenship: United Kingdom

Residence Address: Santa Clara, California

Post Office Address: 550 Mansion Park Drive, #205, Santa Clara, CA 95054

Fourth Inventor's Full Name: James (First) P. (Initial) Kimball (Last)

Inventor's Signature: James P. Kimball

Date: December 9, 1999 Country of Citizenship: USA

Residence Address: San Jose, California

Post Office Address: 15123 Stratford Drive, San Jose, CA 95124

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Fifth Inventor's Full Name: Helmut (First) (Initial) Puchner (Last)

Inventor's Signature:

Date: Dec 07, 1999 Country of Citizenship: Austria

Residence Address: Santa Clara, California

Post Office Address: 3457 Cooper Drive, Santa Clara, CA 95051 USA

Sixth Inventor's Full Name: Ravindra (First) Manohar (Initial) Kapre (Last)

Inventor's Signature: RMKapre

Date: Dec 13, 1999 Country of Citizenship: India

Residence Address: San Jose, California

Post Office Address: 3339 Bel Mira Way, San Jose, CA 95135 USA

Seventh Inventor's Full Name: Nicholas (First) (Initial) Eib (Last)

Inventor's Signature:

Date: Dec 10, 1999 Country of Citizenship: USA

Residence Address: San Jose, California

Post Office Address: 781 Almondwood Way, San Jose, CA 95120 USA